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1 Complete logical routings in computer mail systems

P. Martin, D. Tsichritzis

January 1986 **ACM Transactions on Information Systems (TOIS)**, Volume 4 Issue 1

Publisher: ACM Press

Full text available: pdf(1.16 MB) Additional Information: full citation, abstract, references, index terms, review

The logical routing of a message in a computer mail system involves the identification and location of the set of intended recipients for that message. This function is carried out by the naming and addressing mechanism of the mail system. An important property of that mechanism is that it should be able to identify and locate all the intended recipients of a message, so that, once submitted, a message will not become lost or stuck in the system. We first discuss me ...

2 Address-Indexed Memory Disambiguation and Store-to-Load Forwarding

Sam S. Stone, Kevin M. Woley, Matthew I. Frank

November 2005 **Proceedings of the 38th annual IEEE/ACM International Symposium on Microarchitecture MICRO 38**

Publisher: IEEE Computer Society

Full text available: pdf(301.30 KB) Publisher Site Additional Information: full citation, abstract, index terms

This paper describes a scalable, low-complexity alternative to the conventional load/store queue (LSQ) for superscalar processors that execute load and store instructions speculatively and out-of-order prior to resolving their dependences. Whereas the LSQ requires associative and age-prioritized searches for each access, we propose that an address-indexed store-forwarding cache (SFC) perform store-to-load forwarding and that an address-indexed memory disambiguation table (MDT) perform memory dis ...

3 Complete answer aggregates for treelike databases: a novel approach to combine querying and navigation

Holger Meuss, Klaus U. Schulz

April 2001 **ACM Transactions on Information Systems (TOIS)**, Volume 19 Issue 2

Publisher: ACM Press

Full text available: pdf(356.60 KB) Additional Information: full citation, abstract, references, citings, index terms

The use of markup languages like SGML, HTML or XML for encoding the strucutre of

documents or linguistic data has lead to many databases where entries are adequately described as trees. In this context querying formalisms are interesting that offer the possiblity to refer both to textual content and logical structure. We consider models where the strucutre specified in a query is not only used as a filter, but also for selecting and presenting different parts of the data. If answers are formaliz ...

Keywords: SGML, XML, answer presentation, information retrieval, logic, query languages, semistructured data, structured documents, tree databases, tree matching

4 Toward a complete transformational toolkit for compilers

J. A. Bergstra, T. B. Dinesh, J. Field, J. Heering

September 1997 **ACM Transactions on Programming Languages and Systems (TOPLAS)**, Volume 19 Issue 5

Publisher: ACM Press

Full text available: pdf(525.75 KB) Additional Information: full citation, abstract, references, citings, index terms, review

PIM is an equational logic designed to function as a "transformational toolkit" for compilers and other programming tools that analyze and manipulate imperative languages. It has been applied to such problems as program slicing, symbolic evaluation, conditional constant propagation, and dependence analysis. PIM consists of the untyped lambda calculus extended with an algebraic data type that characterizes the behavior of lazy stores and generalized conditionals. A graph form of ...

Keywords: compiler intermediate representation, completion, imperative language, partial evaluation, program transformation, term-rewriting

5 High-speed prefix-preserving IP address anonymization for passive measurement systems

Ramaswamy Ramaswamy, Tilman Wolf

February 2007 **IEEE/ACM Transactions on Networking (TON)**, Volume 15 Issue 1

Publisher: IEEE Press

Full text available: pdf(1.04 MB) Additional Information: full citation, abstract, references, index terms

Passive network measurement and packet header trace collection are vital tools for network operation and research. To protect a user's privacy, it is necessary to anonymize header fields, particularly IP addresses. To preserve the correlation between IP addresses, prefix-preserving anonymization has been proposed. The limitations of this approach for a high-performance measurement system are the need for complex cryptographic computations and potentially large amounts of memory. We propose a ...

Keywords: anonymization, network measurement, privacy

6 Streamlining data cache access with fast address calculation

Todd M. Austin, Dionisios N. Pnevmatikatos, Gurindar S. Sohi

May 1995 **ACM SIGARCH Computer Architecture News , Proceedings of the 22nd annual international symposium on Computer architecture ISCA '95**, Volume 23 Issue 2

Publisher: ACM Press

Full text available: pdf(1.58 MB) Additional Information: full citation, abstract, references, citings, index terms

For many programs, especially integer codes, untolerated load instruction latencies account for a significant portion of total execution time. In this paper, we present the

design and evaluation of a fast address generation mechanism capable of eliminating the delays caused by effective address calculation for many loads and stores.Our approach works by predicting early in the pipeline (part of) the effective address of a memory access and using this predicted address to speculatively access the ...

7 Power-optimal encoding for DRAM address bus (poster session)

Wei-Chung Cheng, Massoud Pedram

August 2000 **Proceedings of the 2000 international symposium on Low power electronics and design ISLPED '00**

Publisher: ACM Press

Full text available: pdf(207.02 KB) Additional Information: full citation, abstract, references, citings, index terms

This paper presents Pyramid code, an optimal code for transmitting sequential addresses over a DRAM bus. Constructed by finding an Eulerian cycle on a complete graph, this code is optimal for conventional DRAM in the sense that it minimizes the switching activity on the time-multiplexed address bus from CPU to DRAM. Experimental results on a large number of testbenches with different characteristics (i.e. sequential vs. random memory access behaviors) are reported and demonstrate a reductio ...

8 Architecture/power: Power efficient branch prediction through early identification of branch addresses

Chengmo Yang, Alex Orailoglu

October 2006 **Proceedings of the 2006 international conference on Compilers, architecture and synthesis for embedded systems CASES '06**

Publisher: ACM Press

Full text available: pdf(247.99 KB) Additional Information: full citation, abstract, references, index terms

Ever increasing performance requirements have elevated deeply pipelined architectures to a standard even in the embedded processor domain, requiring the incorporation of dynamic branch prediction subsystems to hide the execution latency of control-altering instructions. In this paper a low power early branch identification technique which enables the design of extremely power-efficient branch predictors and BTBs is proposed. Through static extraction of program information regarding the distance ...

Keywords: application-specific processors, dynamic branch prediction, low-power design

9 ATUM: a new technique for capturing address traces using microcode

A. Agarwal, R. L. Sites, M. Horowitz

June 1986 **ACM SIGARCH Computer Architecture News , Proceedings of the 13th annual international symposium on Computer architecture ISCA '86**, Volume 14 Issue 2

Publisher: IEEE Computer Society Press, ACM Press

Full text available: pdf(894.10 KB) Additional Information: full citation, abstract, references, citings, index terms

Trace-driven simulation is often used in the design of computer systems, especially caches and translation lookaside buffers. Capturing address traces to drive such simulations has been problematic, often involving 1000:1 software overhead to trace a target workload, and/or mechanisms that cause significant distortions in the recorded data. A new technique for capturing address traces has been developed to use a processor's microcode to record addresses in a reserved part of main memory as ...

10 An address translation simulator

Steven Robbins

February 2005 **ACM SIGCSE Bulletin , Proceedings of the 36th SIGCSE technical**

symposium on Computer science education SIGCSE '05, Volume 37 Issue 1
Publisher: ACM Press
Full text available: pdf(141.46 KB) Additional Information: full citation, abstract, references, index terms

Virtual memory is a major topic in undergraduate operating systems courses. One aspect of virtual memory, address translation, is often covered in an abstract way. When examples are given, only a piece of the translation is done, using a small translation lookaside buffer or a small single-level page table. Since most students learn best by doing rather than watching, the topic is best understood by having students do realistic address translations. This is problematic since it involves lookup f ...

Keywords: address translation, operating systems, virtual memory

11 Architectural support for translation table management in large address space machines

Jerry Huck, Jim Hays
May 1993 **ACM SIGARCH Computer Architecture News , Proceedings of the 20th annual international symposium on Computer architecture ISCA '93**, Volume 21 Issue 2
Publisher: ACM Press

Full text available: pdf(1.34 MB) Additional Information: full citation, abstract, references, citings, index terms

Virtual memory page translation tables provide mappings from virtual to physical addresses. When the hardware controlled Translation Lookaside Buffers (TLBs) do not contain a translation, these tables provide the translation. Approaches to the structure and management of these tables vary from full hardware implementations to complete software based algorithms. The size of the virtual address space used by processes is rapidly growing beyond 32 bits of address. As the utilized ad ...

12 CAT—caching address tags: a technique for reducing area cost of on-chip caches

Hong Wang, Tong Sun, Qing Yang
May 1995 **ACM SIGARCH Computer Architecture News , Proceedings of the 22nd annual international symposium on Computer architecture ISCA '95**, Volume 23 Issue 2
Publisher: ACM Press

Full text available: pdf(1.36 MB) Additional Information: full citation, abstract, references, citings, index terms

This paper presents a technique for minimizing chip-area cost of implementing an on-chip cache memory of microprocessors. The main idea of the technique *Caching Address Tags, or CAT cache* for short. The *CAT* cache exploits locality property that exists among addresses of memory references for the purpose of minimizing chip area-cost of address tags. By keeping only a limited number of distinct tags of cached data rather than having as many tags as cache lines, the *CAT* ...

13 Compiler construction: an advanced course

F. L. Bauer, F. L. De Remer, M. Griffiths, U. Hill, J. J. Horning, C. H. A. Koster, W. M. McKeeman, P. C. Poole, W. M. Waite, G. Goos, J. Hartmanis
January 1974 Book
Publisher: Springer-Verlag New York, Inc.
Additional Information: full citation, abstract, references, cited by

The Advanced Course took place from March 4 to 15, 1974 and was organized by the Mathematical Institute of the Technical University of Munich and the Leibniz Computing Center of the Bavarian Academy of Sciences, in co-operation with the European Communities, sponsored by the Ministry for Research and Technology of the Federal

Republic of Germany and by the European Research Office, London.

14 Low power techniques for address encoding and memory allocation

Wei-Chung Cheng, Massoud Pedram
January 2001 **Proceedings of the 2001 conference on Asia South Pacific design automation ASP-DAC '01**
Publisher: ACM Press

Full text available: pdf(110.42 KB) Additional Information: full citation, abstract, references, citings, index terms

This paper presents encoding techniques to optimize the switching activity on a multiplexed DRAM address bus. The DRAM switching activity can be classified either as external (between two consecutive addresses) or internal (between the row and column addresses of the same address). To eliminate the external switching activity for sequential access, we propose an optimal encoding, Pyramid code, for conventional DRAM mode as well as Burst Pyramid code for burst mode DRAM. To minimize the inte ...

15 Trace-driven memory simulation: a survey

Richard A. Uhlig, Trevor N. Mudge
June 1997 **ACM Computing Surveys (CSUR)**, Volume 29 Issue 2
Publisher: ACM Press

Full text available: pdf(636.11 KB) Additional Information: full citation, abstract, references, citings, index terms, review

As the gap between processor and memory speeds continues to widen, methods for evaluating memory system designs before they are implemented in hardware are becoming increasingly important. One such method, trace-driven memory simulation, has been the subject of intense interest among researchers and has, as a result, enjoyed rapid development and substantial improvements during the past decade. This article surveys and analyzes these developments by establishing criteria for evaluating trac ...

Keywords: TLBs, caches, memory management, memory simulation, trace-driven simulation

16 A programming language

Kenneth E. Iverson
January 1962 Book
Publisher: John Wiley & Sons, Inc.
Additional Information: full citation, abstract, references, cited by, index terms

From the Preface

Applied mathematics is largely concerned with the design and analysis of explicit procedures for calculating the exact or approximate values of various functions. Such explicit procedures are called algorithms or programs. Because an effective notation for the description of programs exhibits considerable syntactic structure, it is called a programming language.

Much of applied mathematics, particularly the more recent computer-related areas which ...

17 Scalable Load and Store Processing in Latency Tolerant Processors

Amit Gandhi, Haitham Akkary, Ravi Rajwar, Srikanth T. Srinivasan, Konrad Lai

May 2005 **ACM SIGARCH Computer Architecture News , Proceedings of the 32nd annual international symposium on Computer Architecture ISCA '05**, Volume 33 Issue 2

Publisher: IEEE Computer Society, ACM Press

Full text available: pdf(187.74 KB) Additional Information: full citation, abstract, cited by, index terms

Memory latency tolerant architectures support thousands of in-flight instructions without scaling cycle-critical processor resources, and thousands of useful instructions can complete in parallel with a miss to memory. These architectures however require large queues to track all loads and stores executed while a miss is pending. Hierarchical designs alleviate cycle time impact of these structures but the CAM and search functions required to enforce memory ordering and provide data forwarding pl ...

18 Implementing a family of distributed garbage collectors

Stuart Norcross, Ron Morrison, Dave Munro, Henry Detmold

February 2003 **Proceedings of the 26th Australasian computer science conference - Volume 16 ACSC '03**

Publisher: Australian Computer Society, Inc.

Full text available: pdf(353.94 KB) Additional Information: full citation, abstract, references, citings, index terms

This paper discusses implementations of distributed garbage collectors derived using a methodology developed previously that involves mappings of distributed termination detection algorithms (DTAs) to local garbage collection schemes. Implementations produced by such mappings preserve the safety and completeness properties of the original local collectors. Through our collector implementations we have come to understand that the derivation technique extends to distributed collection schemes with ...

Keywords: distributed termination, garbage collection

19 Evaluation of architectural support for global address-based communication in large-scale parallel machines

Arvind Krishnamurthy, Klaus E. Schauser, Chris J. Scheiman, Randolph Y. Wang, David E. Culler, Katherine Yelick

October 1996 **ACM SIGOPS Operating Systems Review , ACM SIGPLAN Notices , Proceedings of the seventh international conference on Architectural support for programming languages and operating systems ASPLOS-VII**, Volume 30 , 31 Issue 5 , 9

Publisher: ACM Press

Full text available: pdf(1.42 MB) Additional Information: full citation, abstract, references, citings, index terms

Large-scale parallel machines are incorporating increasingly sophisticated architectural support for user-level messaging and global memory access. We provide a systematic evaluation of a broad spectrum of current design alternatives based on our implementations of a global address language on the Thinking Machines CM-5, Intel Paragon, Meiko CS-2, Cray T3D, and Berkeley NOW. This evaluation includes a range of compilation strategies that make varying use of the network processor; each is optimiz ...

20 Session: file and access structures: A dynamic address computation mechanism for use in database management

Thomas J. Cook

May 1978 **Proceedings of the 1978 ACM SIGMOD international conference on management of data SIGMOD '78**

Publisher: ACM Press

Full text available: pdf(1.17 MB) Additional Information: full citation, abstract, references

A dynamic address computation mechanism for use in database management is presented. The address computation technique allows information structured according to a given pre-defined tree to be stored without any address pointers, yet the populated tree is assumed to have an arbitrary number of branches below non-terminating tree nodes, and have arbitrary length information stored at the tree leaves. The address computation is accomplished using a compact (yet complete) address-free description o ...

Keywords: address computation, computer architecture, database management systems, segmented-page storage, trees

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Results for "((address<in>metadata) <and> (completion<in>metadata))" e-mail
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» Key

IEEE JNL	IEEE Journal or Magazine
IET JNL	IET Journal or Magazine
IEEE CNF	IEEE Conference Proceeding
IET CNF	IET Conference Proceeding
IEEE STD	IEEE Standard

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Computer Design, 2001. ICCD 2001. Proceedings. 2001 International Confere
23-26 Sept. 2001 Page(s):24 - 29
Digital Object Identifier 10.1109/ICCD.2001.954999
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Heger, D.A.; Simco, G.;
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